REMARKS

Claims 1 through 24 are currently pending in the application.

This amendment is in response to the Office Action of October 21, 2004.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on Ono et al. (U.S. Patent 3,861,969)

Claims 1, 2, 4, 7, 8, 13, 14, 16, 19 and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Ono et al. (U.S. Patent 3,861,969).

Applicant asserts that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Turning to the cited prior art, the Ono et al. reference describes a semiconductor substrate having an Si_3N_4 layer covered by a phosphosilicate glass layer thereon when formed as a double layer serving as a protective layer and/or mask for selective diffusion to avoid a warping of the substrate. A Zn diffusion layer 45 is formed on the back side of a silicon crystal substrate 31 which is removed therefrom by the lapping of the Zn diffusion layer 45 from the substrate 31. The Ono et al. reference does not describe, either expressly or inherently, anything but the removal of the Zn diffusion layer 45 and the formation of a metal 46 which forms an ohmic contact with the n-type semiconductor bonded to the back surface of the substrate by conventional electroless plating. The metal 46 forming an ohmic contact is not described as acting as a stress balancing layer such as Zn diffusion layer 45.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Applicants assert that Ono et al. does not and cannot anticipate the presently claimed inventions of presently amended independent claims 1 and 13 or independent claims 7 and 19 under 35 U.S.C. § 102 because Ono et al. does not identically describe, either expressly or inherently, each and every element of the presently claimed inventions in as complete detail as is

contained in the claims. Specifically, Applicants assert that Ono et al. does not identically describe the elements of the presently claimed inventions of presently amended independent claims 1 and 13 calling for "a passivation layer covering a portion of said integrated circuit causing a stress on at least a portion of the semiconductor substrate" and "a stress-balancing layer covering at least a portion of said back side substantially balancing the stress caused by the front side passivation layer covering a portion of said integrated circuit" or the claimed inventions of independent claims 7 and 19 calling for "a passivation layer covering a portion of said integrated circuit exerting a stress on said substrate front side", "a stress-balancing layer covering at least a portion of said back side, said stress-balancing layer for balancing a portion of said front side stress with a generally equivalent back side stress", "a passivation layer covering a portion of said integrated circuit causing a force acting on a portion of said substrate front side", and "a force-balancing layer covering at least a portion of said back side, said force-balancing layer for balancing a portion of said force on said front side". Applicants assert that, at best, Ono et al describes a local ohmic contact located on the back surface of the substrate to be used as an electrical contact for the n-type semiconductor material. Such is not the claimed inventions of independent claims 1, 7, 13, and 19.

Therefore, since Ono et al. does not describe, either expressly or inherently, the elements of the claimed inventions of independent claims 1, 7, 13, and 19 to anticipate the claimed inventions under 35 U.S.C. § 102, such claims are allowable as well as dependent claims 2 through 6, 8 through 12, 14 through 18, and 20 through 24 therefrom.

Anticipation Rejection Based on Yamauchi (JP 59-132153)

Claims 1 through 24 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yamauchi (JP 59-132153).

Applicants assert that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Turning to Yamauchi, described is a solder blocking region at both end parts of a metalized layer at the back side of the dielectric substrate to limit the soldering area of the substrate to a heat radiating plate to reduce the yield of stress to a dielectric substrate due to temperature change due to the different coefficients of thermal expansion of the dielectric substrate and the heat radiating plate not being equal inducing stress into the dielectric substrate.

Applicants assert that Yamauchi does not and cannot anticipate the presently claimed inventions of presently amended independent claims 1 and 13 or independent claims 7 and 19 under 35 U.S.C. § 102 because Yamauchi does not identically describe, either expressly or inherently, each and every element of the presently claimed inventions in as complete detail as is contained in the claims. Specifically, Applicants assert that Yamauchi does not identically describe the elements of the presently claimed inventions of presently amended independent claims 1 and 13 calling for "a passivation layer covering a portion of said integrated circuit causing a stress on at least a portion of the semiconductor substrate" and "a stress-balancing layer covering at least a portion of said back side substantially balancing the stress caused by the front side passivation layer covering a portion of said integrated circuit" or the claimed inventions of independent claims 7 and 19 calling for "a passivation layer covering a portion of said integrated circuit exerting a stress on said substrate front side", "a stress-balancing layer covering at least a portion of said back side, said stress-balancing layer for balancing a portion of said front side stress with a generally equivalent back side stress", "a passivation layer covering a portion of said integrated circuit causing a force acting on a portion of said substrate front side", and "a force-balancing layer covering at least a portion of said back side, said force-balancing layer for balancing a portion of said force on said front side". Applicants assert that, at best, Yamauchi describes a solder blocking region at both end parts of a metalized layer at the back side of the dielectric substrate to limit the soldering area of the substrate to a heat radiating plate. Such is not the claimed inventions of independent claims 1, 7, 13, and 19.

Therefore, since Yamauchi does not describe, either expressly or inherently, the elements of the claimed inventions of independent claims 1, 7, 13, and 19 to anticipate the claimed inventions under 35 U.S.C. § 102, such claims are allowable as well as dependent claims 2 through 6, 8 through 12, 14 through 18, and 20 through 24 therefrom.

Anticipation Rejection Based on Linn et al. (U.S. Patent 5,728,624)

Claims 1 through 24 were rejected under 35 U.S.C. § 102(b) as being anticipated by Linn et al. (U.S. Patent 5,728,624).

Applicants assert that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Turing to Linn et al., described is low temperature wafer bonding using a silicon-oxidizing bonding liquid to permit the introduction of radiation hardening dopants and electrically active dopants as constituents of the bonding liquid to provide better stress compensation by providing dopants in the bonding liquid which will produce a bonding layer which closely matches coefficients of thermal expansion to that of the substrate wafers.

Applicants assert that Linn et al. does not and cannot anticipate the presently claimed inventions of presently amended independent claims 1 and 13 or independent claims 7 and 19 under 35 U.S.C. § 102 because Linn et al. does not identically describe, either expressly or inherently, each and every element of the presently claimed inventions in as complete detail as is contained in the claims. Specifically, Applicants assert that Linn et al does not identically describe the elements of the presently claimed inventions of presently amended independent claims 1 and 13 calling for "a passivation layer covering a portion of said integrated circuit causing a stress on at least a portion of the semiconductor substrate" and "a stress-balancing layer covering at least a portion of said back side substantially balancing the stress caused by the front side passivation layer covering a portion of said integrated circuit" or the claimed inventions of independent claims 7 and 19 calling for "a passivation layer covering a portion of said integrated circuit exerting a stress on said substrate front side", "a stress-balancing layer covering at least a portion of said back side, said stress-balancing layer for balancing a portion of said front side stress with a generally equivalent back side stress", "a passivation layer covering a portion of said integrated circuit causing a force acting on a portion of said substrate front side", and "a force-balancing layer covering at least a portion of said back side, said force-balancing layer for

balancing a portion of said force on said front side". Applicants assert that, at best, Linn et al describes of radiation hardening dopants and electrically active dopants as constituents of the bonding liquid to provide better stress compensation by providing dopants in the bonding liquid which will produce a bonding layer which closely matches coefficients of thermal expansion to that of the substrate wafers. Such is not the claimed inventions of independent claims 1, 7, 13, and 19.

Therefore, since Linn et al. does not describe, either expressly or inherently, the elements of the claimed inventions of independent claims 1, 7, 13, and 19 to anticipate the claimed inventions under 35 U.S.C. § 102, such claims are allowable as well as dependent claims 2 through 6, 8 through 12, 14 through 18, and 20 through 24 therefrom.

Anticipation Rejection Based on Yamazaki et al. (U.S. Patent 6,380,558)

Claims 1 through 24 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yamazaki et al. (U.S. Patent 6,380,558).

Applicants assert that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Turning to Yamazake et al., described is a semiconductor device having a first insulating layer 102 formed on a substrate 101 having an insulating surface. A silicon nitride oxide film 102b is provided between the silicon nitride oxide film 102a and an active layer 103 on the upper surface of the substrate 101 so as to slightly relieve the action of stress.

Applicants assert that Yamazake et al does not and cannot anticipate the presently claimed inventions of presently amended independent claims 1 and 13 or independent claims 7 and 19 under 35 U.S.C. § 102 because Yamazake et al does not identically describe, either expressly or inherently, each and every element of the presently claimed inventions in as complete detail as is contained in the claims. Specifically, Applicants assert that Yamazake et al does not identically describe the elements of the presently claimed inventions of presently amended independent claims 1 and 13 calling for "a passivation layer covering a portion of said

integrated circuit causing a stress on at least a portion of the semiconductor substrate" and "a stress-balancing layer covering at least a portion of said back side substantially balancing the stress caused by the front side passivation layer covering a portion of said integrated circuit" or the claimed inventions of independent claims 7 and 19 calling for "a passivation layer covering a portion of said integrated circuit exerting a stress on said substrate front side", "a stress-balancing layer covering at least a portion of said back side, said stress-balancing layer for balancing a portion of said front side stress with a generally equivalent back side stress", "a passivation layer covering a portion of said integrated circuit causing a force acting on a portion of said substrate front side", and "a force-balancing layer covering at least a portion of said back side, said force-balancing layer for balancing a portion of said force on said front side". Applicants assert that, at best, Yamazake et al describes a silicon nitride oxide film 102b is provided between the silicon nitride oxide film 102a and an active layer 103 on the upper surface of the substrate 101 so as to slightly relieve the action of stress. Such is not the claimed inventions of independent claims 1, 7, 13, and 19.

Therefore, since Yamazake et al. does not describe, either expressly or inherently, the elements of the claimed inventions of independent claims 1, 7, 13, and 19 to anticipate the claimed inventions under 35 U.S.C. § 102, such claims are allowable as well as dependent claims 2 through 6, 8 through 12, 14 through 18, and 20 through 24 therefrom.

Anticipation Rejection Based on Lowack et al. (U.S. Publication No. 2003/0207095)

Claims 1, 7, 13 and 19 were rejected under 35 U.S.C. § 102(e) as being anticipated by Lowack et al. (U.S. Publication No. 2003/0207095).

Applicants assert that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Turing to Lowack et al., described are electronic and microelectonic components having insulating material having physical weaknesses that are either not compensated for or are compensated for by an extra covering, a substrate back coating (e.g. to lessen stress-induced substrate flexion) or another auxiliary structure.

Applicants assert that Lowack et al.does not and cannot anticipate the presently claimed inventions of presently amended independent claims 1 and 13 or independent claims 7 and 19 under 35 U.S.C. § 102 because Lowack et al.does not identically describe, either expressly or inherently, each and every element of the presently claimed inventions in as complete detail as is contained in the claims. Specifically, Applicants assert that Lowack et al.does not identically describe the elements of the presently claimed inventions of presently amended independent claims 1 and 13 calling for "a passivation layer covering a portion of said integrated circuit causing a stress on at least a portion of the semiconductor substrate" and "a stress-balancing layer covering at least a portion of said back side substantially balancing the stress caused by the front side passivation layer covering a portion of said integrated circuit" or the claimed inventions of independent claims 7 and 19 calling for "a passivation layer covering a portion of said integrated circuit exerting a stress on said substrate front side", "a stress-balancing layer covering at least a portion of said back side, said stress-balancing layer for balancing a portion of said front side stress with a generally equivalent back side stress", "a passivation layer covering a portion of said integrated circuit causing a force acting on a portion of said substrate front side", and "a force-balancing layer covering at least a portion of said back side, said force-balancing layer for balancing a portion of said force on said front side". Applicants assert that, at best, Lowack et al. describes as general matter merely states that electronic and microelectonic components having insulating material having physical weaknesses that are either not compensated for or are compensated for by an extra covering, a substrate back coating (e.g. to lessen stress-induced substrate flexion) or another auxiliary structure. Such is not an identical description, either expressly or inherently, of the elements of the claimed inventions of independent claims 1, 7, 13, and 19.

Therefore, since Lowack et al.does not describe, either expressly or inherently, the elements of the claimed inventions of independent claims 1, 7, 13, and 19 to anticipate the claimed inventions under 35 U.S.C. § 102, such claims are allowable as well as dependent claims 2 through 6, 8 through 12, 14 through 18, and 20 through 24 therefrom.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Applicant's Admitted Prior Art shown in Figure 2B in view of Hilt et al. (U.S. Publication No. 2003/0017626)

Claims 1, 2, 4, 7, 8, 13, 14, 16, 19 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art shown in Figure 2B in view of Hilt et al. (U.S. Publication No. 2003/0017626). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants assert that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Turning to the cited prior art, Hilt et al. teaches or suggests that a distorting material 70 may be applied to the back side of a wafer substrate 22 at room temperature which causes the wafer substrate to deform during the growth of epitaxial layers on the front side of the wafer substrate so that the strain caused by the epitaxial layers on the front side of the wafer substrate results in the wafer substrate being generally planar. Further, after the growth of the epitaxial layers on the front side of the wafer substrate, the distorting material applied to the back of the wafer substrate 22 may be removed.

Applicants assert that any combination of the Applicants' admitted prior art and Hilt et al. do not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 7, 13 and 19 because, at the least, any combination of Applicants' admitted prior art and Hilt et al. does not teach or suggest all of the claim limitations thereof.

Applicants assert that any combination of the cited prior art does not and cannot teach or suggest the claim limitations of the presently claimed inventions of presently amended independent claims 1 and 13 or independent claims 7 and 19 under 35 U.S.C. § 103 claims 1 and 13 calling for "a passivation layer covering a portion of said integrated circuit causing a stress on at least a portion of the semiconductor substrate" and "a stress-balancing layer covering at least a portion of said back side substantially balancing the stress caused by the front side passivation layer covering a portion of said integrated circuit" or the claimed inventions of independent claims 7 and 19 calling for "a passivation layer covering a portion of said integrated circuit exerting a stress on said substrate front side", "a stress-balancing layer covering at least a portion of said back side, said stress-balancing layer for balancing a portion of said front side stress with a generally equivalent back side stress", "a passivation layer covering a portion of said integrated circuit causing a force acting on a portion of said substrate front side", and "a force-balancing layer covering at least a portion of said back side, said force-balancing layer for balancing a portion of said force on said front side". Applicants assert that, at best, any combination of the cited prior art teaches or suggests the use of a distorting material that may be applied to the back side of a wafer substrate at room temperature which causes the wafer substrate to deform during the growth of epitaxial layers on the front side of the wafer substrate so that the strain caused by the epitaxial layers on the front side of the wafer substrate results in the wafer substrate being generally planar. Further, after the growth of the epitaxial layers on the front side of the wafer substrate, the distorting material applied to the back of the wafer substrate 22 may be removed. Such is not the claim limitations of the claimed inventions of independent claims 1, 7, 13, and 19.

Therefore, since any combination of the cited prior art does not teach or suggest the claim limitations of the claimed inventions of independent claims 1, 7, 13, and 19 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions, independent claims 1, 7, 13, and 19 are allowable as well as dependent claims 2 through 6, 8 through 12, 14 through 18, and 20 through 24 therefrom.

In summary, for the reasons set forth herein, Applicants submit that claims 1 through 24 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 1 through 24 and the case passed for issue.

Respectfully submitted,

James R. Duzan
Registration No. 28,393
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: January 20, 2005
JRD/dlm:lmh

Document in ProLaw